SOME DESIGN TECHNIQUES AND CONSIDERATIONS FOR A JUNCTION TRANSISTOR FLIP-FLOP

DAVID D. KILPATRICK

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by

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PREFACE

The work and study from which this paper emerged was performed during the first three months of 1955, during an industrial tour with the National Cash Register Company, Electronics Division, located at Hawthorne, California.

The effort expended during this tour was directed primarily toward completion of the first phase of a study program concerned with junction transistor flip-flops. Considered to be of fundamental importance in this phase was the development of design techniques for junction transistor flip-flop circuits employing commercially available transistors and associated components, and based upon the inherent advantages and limitations of junction transistors. It is felt that this phase reached its logical conclusion with the evolution of the graphical method described herein.

The writer wishes to thank Seymour Schoen, of the National Cash Register Company, for his efforts in setting up the program and for his critical review of the results.

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LIST OF ILLUSTRATIONS

TABLE OF SYMBOLS

Cl	Value of "speed-up" capacitor (Figure 4).
Ebb	Value of base bias voltage (Figure 2).
Ecc	Value of supply voltage (Figure 4).
Ib	Value of current in the transistor base circuit.
Ibo	Value of current in the base circuit when the transistor is cut-off.
Ic	Value of collector current when the transistor is conducting.
Ico	Value of collector current when the transistor is off.
Ie	Value of current in the emitter circuit.
Rx	Value of various resistors (Figures 4 and 11).
To	The period of time for the collector current to reach 90% of its saturation value. Called "turn on" time (Figure 3).
Ts	The period of time from reaching saturation current level until the turn off event occurs (Figure 3).
Tl	Minority carrier storage time (Figure 3).
T2	Decay time (Figure 3).
α_I	Transistor current gain with the collector functioning as an emitter and the emitter functioning as a collector.
α_N	Transistor current gain with the transistor functioning normally.
ω_I	Cut-off frequency of the "inverted" alpha.
ω_N	Cut-off frequency of the normal alpha.

CHAPTER I

INTRODUCTION

1. Definition.

The IRE Standards on Electronic Computers: Definition of Terms, 1950, [11] defines "flip-flop" as:

> An electronic circuit having two stable states and ordinarily two input terminals (or types of input signals) each of which corresponds with one of the two states. The circuit remains in either state until caused to change to the other state by application of the corresponding signal.

2. Background.

The flip-flop is one of the earliest forms of electronic circuit. The oldest and most widely known flip-flop was described in 1919 by W. H. Eccles and F. W. Jordan in their article "A Trigger Relay Utilizing Three Electrode Thermionic Vacuum Tubes" [3]. The Eccles-Jordan circuit is very widely used today, both in its original form and various modified forms.

Recent advances and emphasis in the digital computer field have increased many fold the number of flip-flops in use. A single computer may easily use hundreds of these circuits since counters and the various types of registers are specialized arrangements of a number of flip-flops.

Due to this great utilization of flip-flops, it is important that the best available device be employed for any particular application. No attempt will be made here to establish the superiority of one device

over another, but it is in order to mention the several devices most commonly used today, with some of their principle characteristics. These are vacuum tubes, ferromagnetic cores and transistors. Some characteristics of these are mentioned below.

(a) Vacuum tube. Recent developments and tube improvement have increased the reliability and life of vacuum tubes. Manufacturers have given particular attention to computer applications and the particular problems created thereby. However, vacuum tubes always require heater power, and in many instances this enabling power will exceed the useful work performed by the tube, thus lowering the device efficiency by a large factor. The vacuum tube also requires large allowances for space and weight. For these reasons, in particular, it appears desirable to supplant the tube in computer applications where several thousand might be in use.

(b) Ferromagnetic core. A typical circuit utilizing this device is described by Carl Isborn in "Ferroresonant Flip-Flops" [4]. The magnetic core is very rugged, has a high degree of reliability and affords a means of constructing a circuit of relatively low power consumption. Their useful frequency coverage is at least through the medium frequency range (100 to 200 KC) which is commonly used. The principle objection to their use is the requirement for an alternating voltage supply.

(c) Transistors. The preface to "Principles of Transistor

Circuits", [8] edited by R. F. Shea, has given a concise description of the transistor:

> The transistor is small, yet extremely rugged, and is capable of withstanding shocks many thousands of times greater than the force of gravity. It consumes no filament power; in fact, the junction transistor is capable of operation at power consumption of the order of a microwatt. Power outputs of the order of watts have been obtained from the earlier forms of transistors. The upper limit of power dissipation, however, is primarily a function of mechanical design, and power outputs of hundreds of watts are not beyond the realm of possibility.... In addition to their low power consumption, transistors operate with low voltage supplies, especially the junction transistor, whose operation at a fraction of a volt is practicable. Finally, and possibly most important, transistors have a long life.

In addition to the features noted above, the point contact transistor has an inherent negative resistance property, which has been described by A. E. Anderson in "Transistors in Switching Circuits" [1]. This negative resistance characteristic makes possible a flip-flop that utilizes a single active element. The point contact transistor is at present the only device capable of such operation. This capability appears to offer a great advantage, but as yet, no scheme has been devised to take full advantage of it since contemporary thinking demands that two outputs as afforded by the Eccles-Jordan circuit be available. In order to provide two outputs, it is necessary to resort to the use of two point contact transistors.

The characteristic of the junction transistor that makes it adaptable for use in flip-flop circuitry is the voltage phase reversal which occurs in the grounded emitter configuration. In this respect,

the transistor is similar to the vacuum tube, and for this reason a transistor circuit configuration of the Eccles-Jordan type is feasible. However, it must be kept in mind that the junction transistor is essentially a current controlled device, rather than a voltage controlled device like the vacuum tube. This is true even though certain voltage criteria must be met for operation of transistors.

In the past few months, the emphasis in transistor technology has shifted almost entirely to the junction transistor. Reasons for this include the fact that a complete understanding of action in the point contact transistor has not yet been achieved. This results in a low degree of designability. Also, the difficulties of mass producing point contact units with similar characteristics have not been overcome. The resulting variability of characteristics makes necessary the use of complex auxiliary circuits to provide for interchangeability of units. However, manufacturers and physicists have retained an interest in the point contact transistor and it appears likely that it will regain some importance in the future. The point contact types will very likely always afford a higher frequency response (and faster switching speeds) than will the junction transistor.

Other types of devices which have been used in flip-flop type circuitry are gas tubes and barium titanates. These will not be discussed here, but are mentioned in order to indicate that the devices described above do not hold a monopoly of application.

CHAPTER II

JUNCTION TRANSISTORS IN SWITCHING APPLICATIONS

1. A switching circuit.

The material of this chapter is not intended to be exhaustive. It is included to provide a sufficient background for clarity of material of the following chapters without further reference. Articles mentioned in the text discuss fully the junction transistor as a switch, but for the present we are interested only in the grounded emitter configuration of junction transistor circuits. The simplest form of grounded emitter circuit is shown in Figure 1.

2. Large signal behavior of junction transistors.

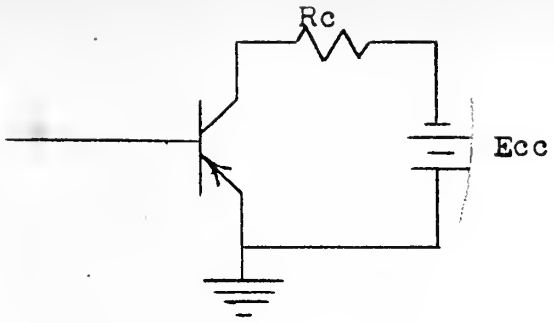
Early analysis of junction transistors in small signal circuits is not applicable to description of their action in switching circuits. However, J. J. Ebers and J. L. Moll in "Large Signal Behavior of Junction Transistors" [2] have sufficiently related the usual small signal parameters to behavior of junction transistors in all circuits, including switching circuits.

Ebers and Moll [2] follow the lead of Anderson [1] in referring to three regions of operation in switching action. These are:

Region I: Collector current cut off,
Region II: Active region,
Region III: Collector current saturation.

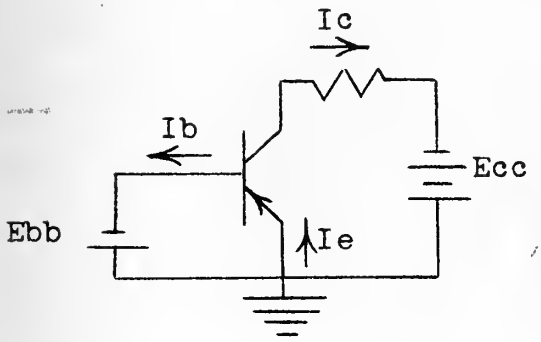
In general the three regions can be identified by bias conditions as:

Region I: Emitter reverse biased, collector reverse biased,
Region II: Emitter forward biased, collector reverse biased,
Region III: Emitter forward biased, collector forward biased.



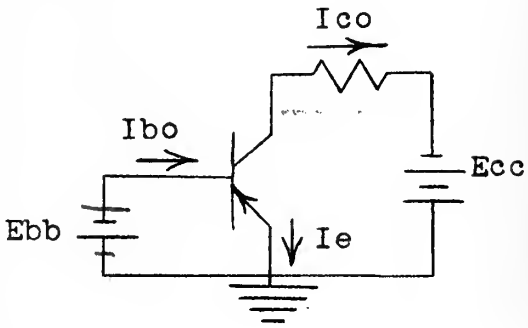
The simplest form of grounded emitter circuit

Figure 1



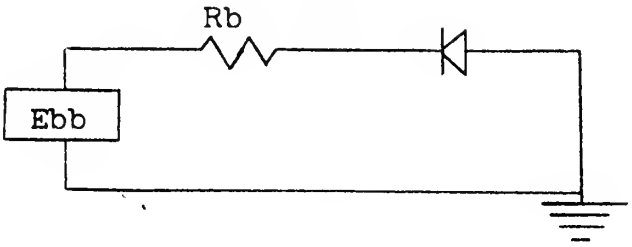
Currents for Regions II and III

(a)



Currents for Region I

(b)



Simplified steady state equivalent base circuit

(c)

Currents in the grounded emitter circuit

Figure 2

In the circuit with which we will be concerned, there is, in effect, means of controlling emitter bias. The condition of bias will determine the amount and direction of current in the base circuit in the manner described below. The base current determines the level of collector current, until the collector current reaches the saturation level. In the saturated condition, the collector current is limited principally by the external circuitry.

3. Base and collector currents.

With the transistor biased for operation in Region II the magnitude of collector current is a direct function of the base current. It is assumed that the reader is familiar with typical grounded-emitter collector characteristics of junction transistors from which such information is obtained.

The boundary between Region I and Region II may be taken as the point at which the emitter current is reduced to zero. For the cut-off condition to exist, it is necessary that the base current actually be reversed from the direction in the active region. It should be recalled that with a p-n junction biased in the reverse direction, the junction presents a high impedance so that any steady state currents are small. These reverse currents are also practically constant with variation in voltage until the Zener voltage is reached, at which point the junction breaks down and current increases quite rapidly. Magnitudes of collector cut-off current, Ico, are commonly less than ten microamperes for good transistors. Use and aging of a

transistor may cause the value to increase to a level many times the original value of a few microamperes. It is therefore desirable that practical circuits be capable of proper operation with transistors having a large range of values of collector cut-off current.

From what has been said above it is apparent that the base circuit might be represented as a simple diode. Figure 2(a) indicates the simplest type of grounded emitter circuit with base and collector currents indicated for Regions II and III. Figure 2(b) indicates the same circuit with currents of Region I. Note that in this case it has been necessary to reverse the base-emitter bias. Figure 2(c) indicates a simplified circuit which might be taken as representative of the base circuit.

At this point it is desirable that some further distinction between operation in Region II and Region III be indicated. Essentially, it is necessary that some minimum value of base current exist in order for the collector current to reach its maximum value, and that with greater magnitudes of base current there be no further increase in collector current. It cannot be said, however, that larger values of base current have no effect. One condition of note which occurs with excess base current is a phenomenon known as "hole storage". In general, "hole storage" is a detrimental effect, resulting from an excess of minority carriers being injected into the base region of the transistor. The greater the amount of this excess, the greater the period of time involved in clearing the base region of minority carriers

when it is desired to switch operation into Region II. In spite of this, it is sometimes advantageous to use large peak base currents in order to obtain more rapid switching times. Also, operation with excess base current for a normal transistor in a particular circuit will allow operation with inferior units at the same level of collector current.

4. Voltage drops across the transistor.

Ebers and Moll [2] have given exact equations for computation of voltage drops across the transistor junctions. For present purposes it is necessary only that the general nature of these voltages be known.

In Region I the p-n junctions are biased in the reverse direction and consequently constitute high impedances. As such, almost all of the applied voltages appear across the transistor.

In Region II the voltage from the emitter to collector may be determined from the collector characteristics, while the base to emitter voltage will approach a value of perhaps one-tenth to five tenths of a volt. The exact voltage is a function of the collector current.

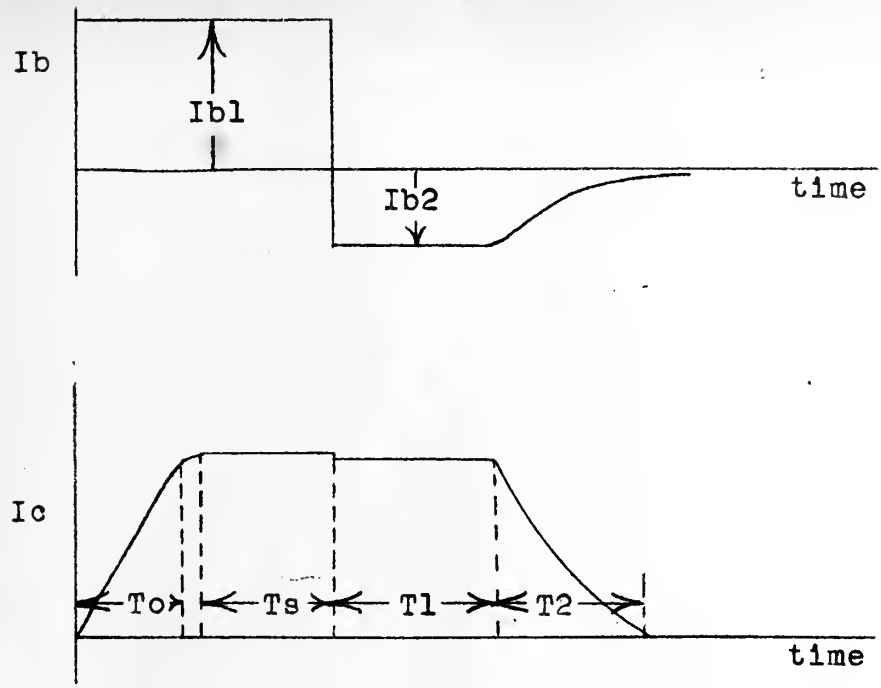
In Region III the base to emitter voltage does not change appreciably from its previous value. The collector to emitter voltage becomes very small and in practical cases can generally be assumed to be zero. Note that the collector to base voltage actually reverses polarity from that of Regions I and II.

5. Switching time.

The time required for the transistor to change from a condition of cut-off to a condition of conduction, and vice-versa, is a matter of primary importance in all switching applications. Ebers and Moll [2] treat this subject, and Moll treats the subject further in "Large Signal Transient Response of Junction Transistors" [6]. The drawing and equations of Figure 3 are taken from this article and are adequate to illustrate the action involved. In Figure 3 note in particular that a relatively large amount of reverse current may flow in the base circuit as long as there is any significant current in the collector circuit. This feature represents a marked departure of behavior in the base circuit from the behavior of a simple diode as indicated in Figure 2(c).

6. Adaptability of transistor types to switching applications.

It is to be noted that most work to the present time has been done with p-n-p type units. The reason for this is that practically all n-p-n transistors have been manufactured by the grown junction techniques, while the p-n-p types have been manufactured by the alloy junction techniques. The significance of this is that the grown types inherently have physically larger emitter and collector regions, and consequently cause the power dissipation in these regions to be greater. Otherwise, the n-p-n may be intrinsically superior due to the minority carriers (which are electrons) having a greater mobility, and, consequently, shorter periods of minority carrier storage.



$$T_o = \frac{1}{(1-\alpha_N)\omega_N} \ln \frac{I_B}{I_B - .9\frac{(1-\alpha_N)}{\alpha_N} I_c}$$

$$T_{s1} = \frac{1}{(1-\alpha_I)\omega_I}$$

$$\text{if } T_s > T_{s1}; \quad T_1 = \frac{\omega_N + \omega_I}{\omega_N \omega_I (1-\alpha_N\alpha_I)} \ln \frac{I_{B1} - I_{B2}}{I_{c1}\left(\frac{1-\alpha_N}{\alpha_N}\right) - I_{B2}}$$

$$\text{if } T_s \ll T_{s1}; \quad T_1 \approx T_s$$

$$T_2 = \frac{1}{(1-\alpha_N)\omega_N} \ln \frac{I_{c1} - \left(\frac{\alpha_N}{1-\alpha_N}\right) I_{B2}}{\frac{1}{10} I_{c1} - \left(\frac{\alpha_N}{1-\alpha_N}\right) I_{B2}}$$

Response to large signal pulse of current in the base circuit

Figure 3

CHAPTER III

JUNCTION TRANSISTOR FLIP-FLOP

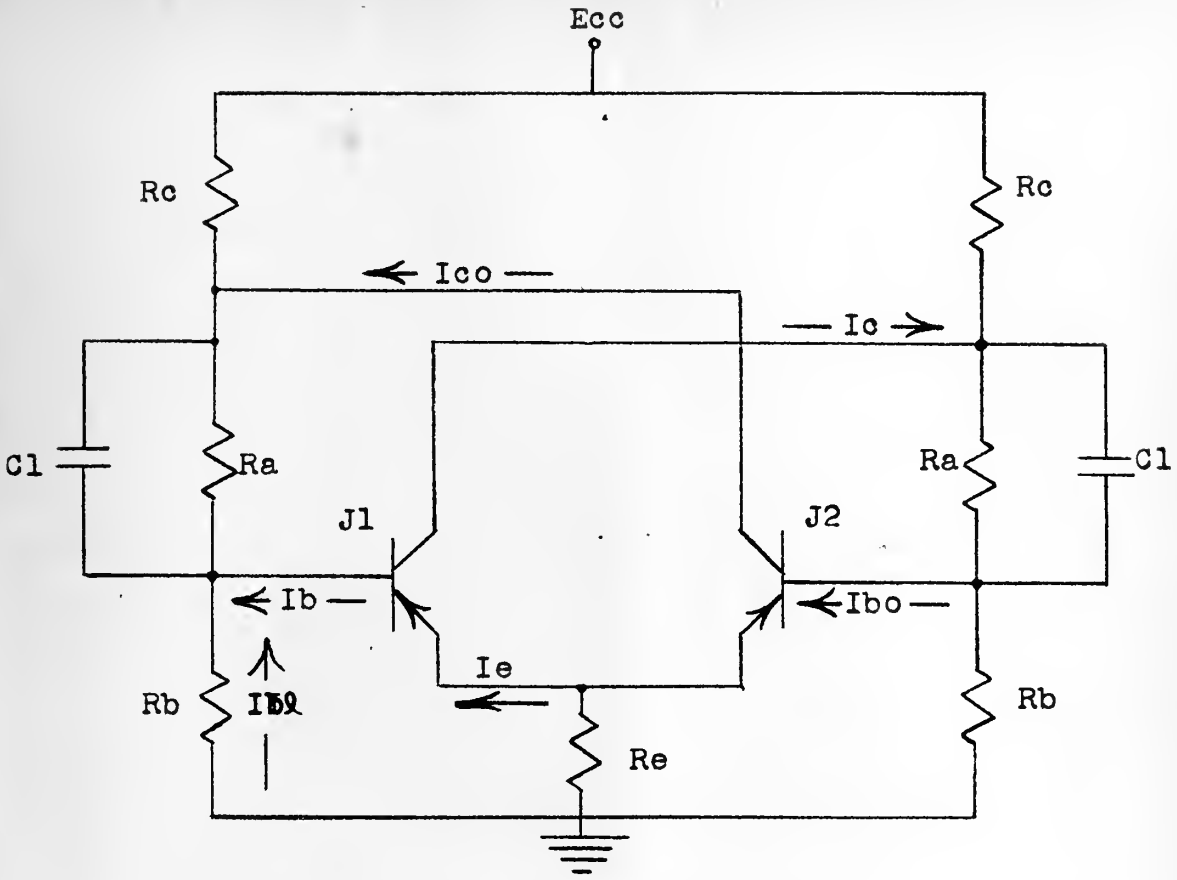
1. Circuit.

A basic type of flip-flop circuit which has proven to be very well adapted to use with the junction transistor is shown in Figure 4. This circuit is identical in configuration to the conventional vacuum tube Eccles-Jordan circuit. It is the only basic configuration considered in this paper.

A point of importance is the polarity of Ecc. With a vacuum tube circuit, the only polarity for the equivalent voltage is positive, but with transistors, Ecc may be either positive or negative depending on whether n-p-n or p-n-p types are being employed. This variation in polarity leads to some possibility of confusion, particularly in discussions of changes in voltage levels. In order that all remarks will be equally applicable to either n-p-n or p-n-p circuits an "increase" in voltage will indicate an actual increase in magnitude, and "decrease" will indicate an actual decrease in magnitude. Another possible point of confusion is in current directions. All currents shown in the figures will be for p-n-p circuits, the equivalent n-p-n currents being opposite.

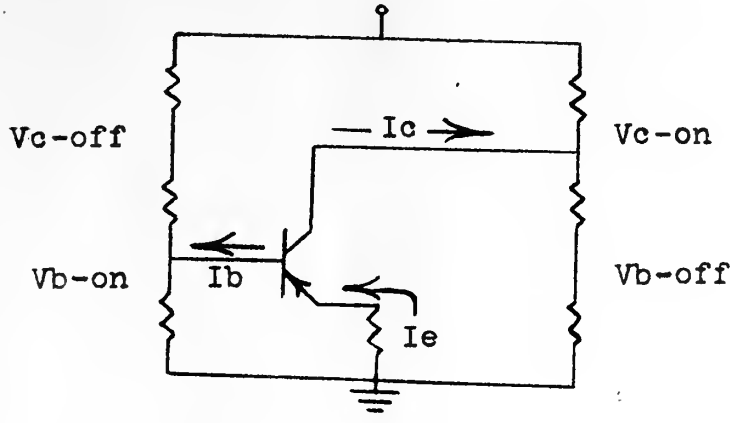
2. Quiescent conditions.

In the circuit of Figure 4, one stable state exists when J1 is conducting and J2 is off; the other stable state exists when J2 is



Basic flip-flop circuit

Figure 4



Simplified steady state circuit

Figure 5

is conducting and J1 is off. The circuit remains in one of these stable states, with no change in currents or voltages until some action occurs to cause the circuit to change to the other stable state.

In Chapter II we have seen the requirements which must be met for a transistor to be in the cut-off condition. The operation of the present circuit is such that current, Ic, in the conducting collector must be sufficiently great that Vb-off is less than Ve. If it is assumed that J2 is off, and is ideal so that it has no leakage current, the circuit of Figure 4 may be redrawn as Figure 5. This circuit emphasizes the interest in Ib and Ic, and Ie since

$$I_e + I_c = I_b$$

Ie will directly determine the quiescent value of Ve. The voltage at the base will be greater than Ve, as pointed out in Chapter II. The voltage that would exist at the base point if the transistor were disconnected must be even greater than this value or no base current will flow at all.

Vc-on is seen to be determined by Ic, and by whatever current is flowing in the lower portion of the resistor network. Usually this latter current is very small compared to the collector current. It should be held in mind here that the value of Ic is dependent upon Ib.

From the foregoing it is seen that all voltages and currents in the circuit are closely inter-related. However, these relationships are well defined such that accurate adjustment of all currents and

voltages is possible. This leads to excellent design control of the circuit.

3. Transition between states.

In the following discussion, Ve will be considered to be constant. This condition holds in practice when use is made of a by-pass capacitor in parallel with Re. When the transition takes place, Vc-on, Vc-off, Vb-on, and Vb-off in Figure 5 will interchange positions appropriately. Ic and Ib will cease to flow as indicated and will finally be flowing at the same level in J2.

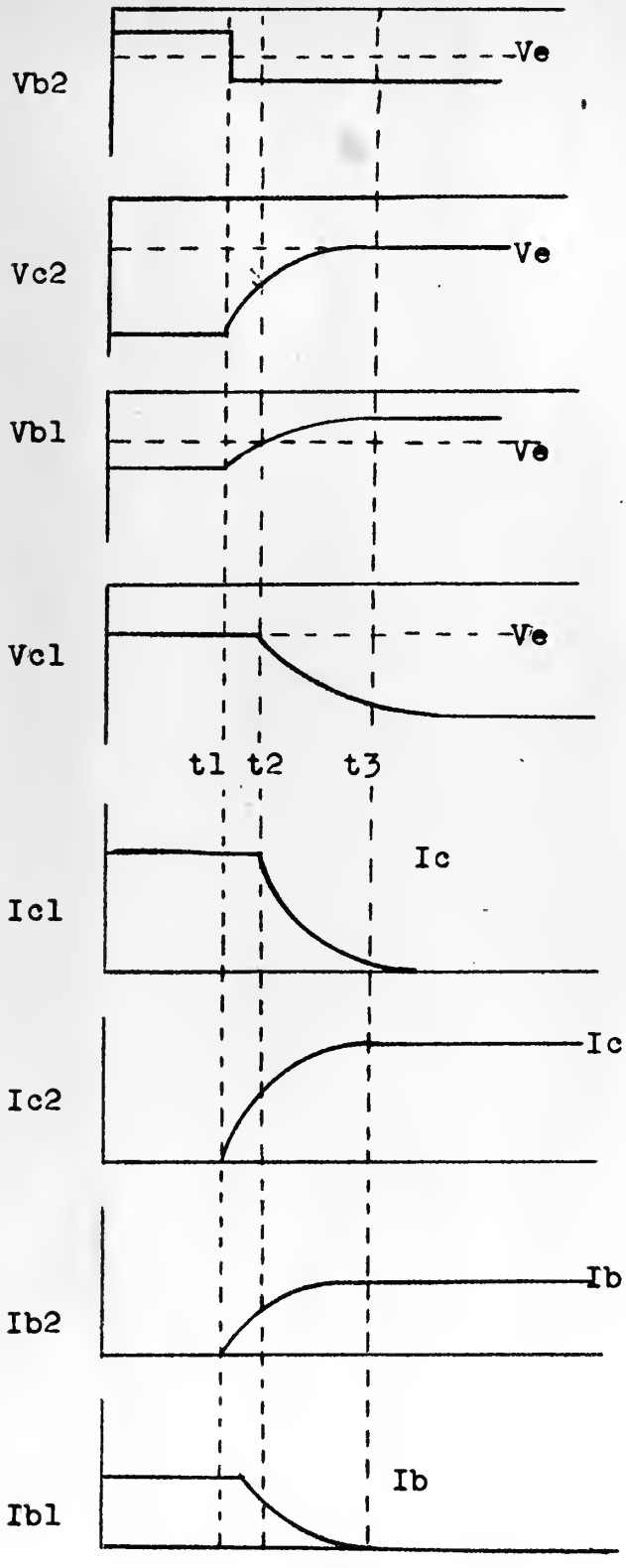
For purposes of this discussion it will be convenient to assume a discontinuity, or unit step, disturbance in some part of the circuit, without considering at this time how the disturbance is introduced. For the present, a unit step of voltage will be assumed to occur at the non-conducting base. In order for this step to have any effect it must be of sufficient magnitude to increase the voltage Vb-off to a value greater than Ve, thus allowing a current to flow in J2. It should now be possible to trace resulting voltage and current changes

around the circuit to show how conditions change to maintain the altered level of Vb-off after the external disturbance has been removed. To facilitate a more complete understanding of how this transition occurs, waveforms of current and voltage have been sketched in Figure 6, and time constants of exponentials have been indicated thereon. For this purpose, the article of Moll [6] previously quoted has been drawn upon for essential information. The waveforms as drawn in Figure 6 are for a p-n-p circuit and a negative value of Ecc. J1 is assumed to be initially conducting.

Since Vb of J2 is assumed to incur a unit step disturbance, this can be drawn without further comment. Result of the change in Vb is an exponentially increasing base current, Ic2. These transitions are pure exponentials if Vb2 incurs a pure unit step.

As Ic2 increases, Vc2 decreases from Vc-off toward Vc-on. If this voltage change were solely a function of Ic2 it would be a pure exponential also. In practice it is found that other effects (particularly changes in Ib1) cause this transition to deviate from exponential. Appendix II illustrates this point more fully.

All of the above events are indicated as commencing at time t1. At time t2, Vc2 is considered to have reached some value, V', which is the level required to reduce Vb1 to a point where J1 begins to cut off. Actually, Ib1 began to decrease at some time between t1 and t2, but there was no change in Ic1 because of excess base current allowed to insure that the transistor was operating in Region III. If the



Time Constants

$\tau = 0$

$$\tau = \frac{1}{(1-\alpha_N)\omega_N}$$

$$\tau = \frac{1}{\left(1-\alpha_N+\frac{r_e}{r_b}\right)\omega_N}$$

$$\tau = \frac{1}{\left(1-\alpha_N+\frac{r_e}{r_b}\right)\omega_N}$$

Waveforms for transition of flip-flop

Figure 6

transistor is not saturated, t1 and t2 tend to occur simultaneously.

At some instance, t3, during the decay of Ic1, a value of Vc1 is reached that is sufficient to maintain Vb2 greater than Ve and conduction will be maintained in J2 if the external voltage is removed.

The foregoing description is purely qualitative. Appendix II gives an approximate solution for the waveforms. The collector voltages do not follow exponentials, and no exact solution for the transition has been obtained. J. R. Tillman in "Transition of an Eccles-Jordan Circuit" [10] has analyzed the vacuum tube circuit to obtain as exact solution, and while his results are not directly applicable to the transistor circuit, it appears possible that the same basic approach might be applied to obtain a solution.

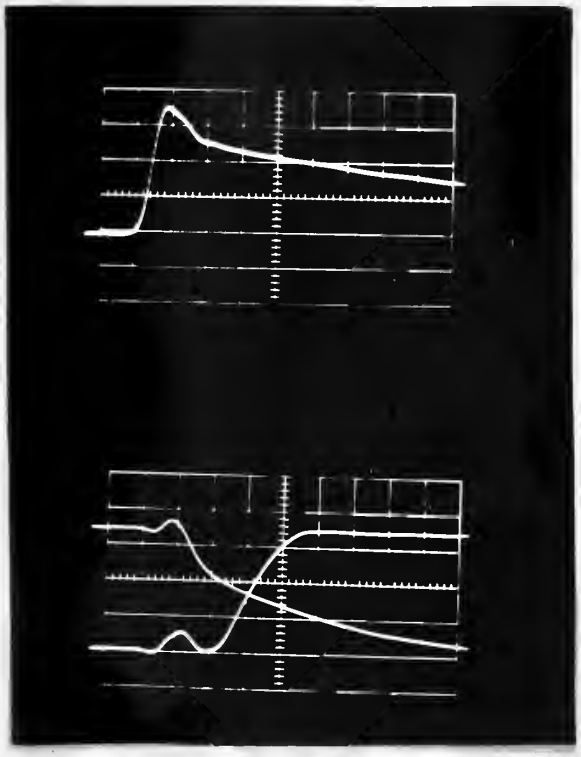
Figure 7 is a photograph of actual waveforms, showing collector voltage transitions and the applied trigger. Figure 8 is a photograph of the base and collector waveforms obtained at a trigger frequency of 500 kilocycles. Figure 9 is a photograph of the collector waveform with two different values of C1 (Figure 4). The circuit from which these waveforms were obtained is indicated in Figure 7, and is the circuit used as a design example in Chapter IV.

Returning to Figure 6, it is important to note the requirement for a finite width of trigger pulse. Also note that no "hole storage" effect has been included here and that such inclusion would demand an even greater trigger width. The effect of the speed-up capacitors, C1 in Figure 4, is ignored in deriving the waveforms of Figure 6

Scale per reticule:

Vertical 2 volts

Horizontal .1 microsecond



Trigger waveform

Collector waveforms

Ra 15 Kohm

Rb 8200 ohm

Rc 2200 ohm

Re 470 ohm

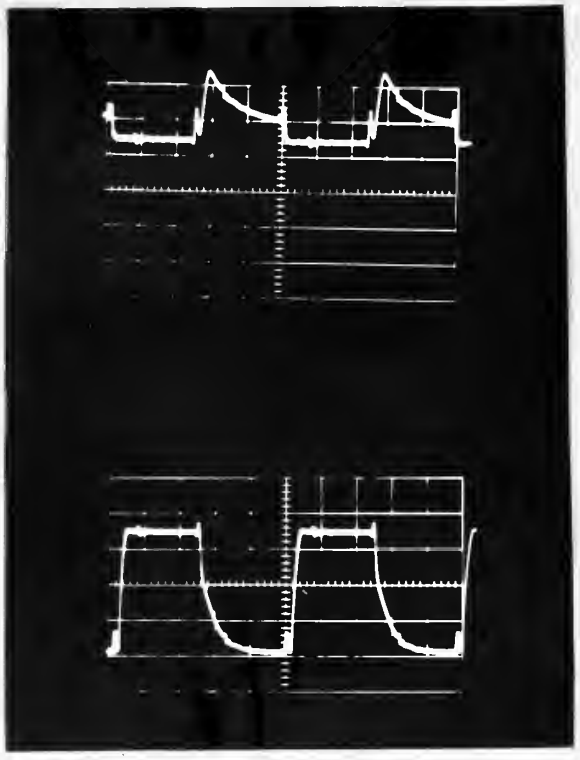
Collector waveforms during transition

Figure 7

Scale per reticule:

Vertical 2 volts

Horizontal 1 microsecond



Base waveform

Collector waveform

Upper limit of each frame is zero volts

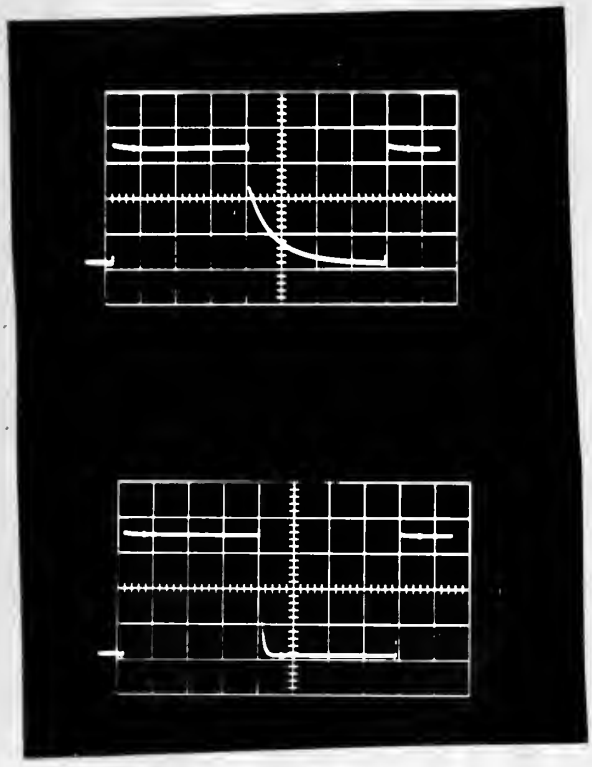
Base and collector waveforms at 500 kilocycles

Figure 8

Scale per reticule:

Vertical 2 volts

Horizontal 2½ microseconds



c1 2000 μμf

c1 150 μμf

Clock frequency: 50 Kilocycles

Collector waveforms showing effect of speed-up capacitor

Figure 9

although these capacitors are essential for proper operation, and have a decided effect upon the ultimate wave shapes as is indicated in Figure 9. The problem of selection of C1 is discussed further in Chapter IV.

4. Triggering methods.

In the discussion above, an increasing step was applied to the non-conducting base. In practice it is found possible to initiate transition in a number of ways, which are:

(a) increasing step to non-conducting base,

(b) decreasing step to conducting base,

(c) increasing step to conducting collector,

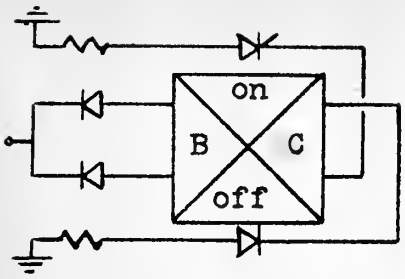
(d) decreasing step to non-conducting collector.

These are in some ways equivalent, since the speed up capacitors couple a voltage change to the collector of the other transistor. Considering the methods as distinctive leads to different configurations of external circuitry, however. The various configurations used as trigger circuits by the writer are shown in Figure 10. The importance of the level of diode bias voltages is not to be overlooked, since these voltages in a large part determine the trigger amplitude required. No analytic solution for trigger voltage and current requirements has been obtained. Some experimental data has been obtained of which that in Appendix I is typical.

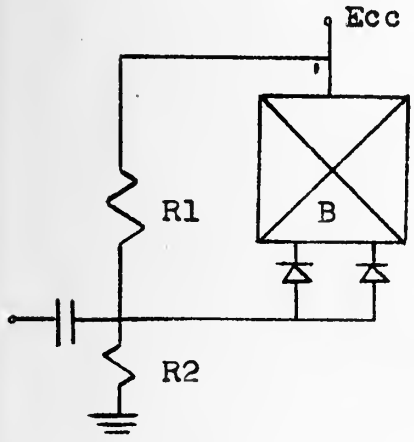
5. Loading.

In order for the circuit to be useful, there must be a convenient

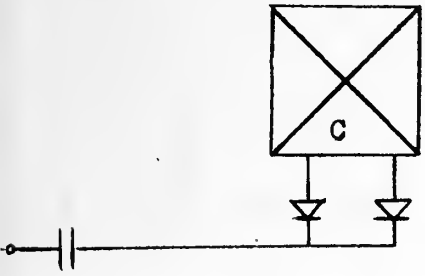
Circuit Action



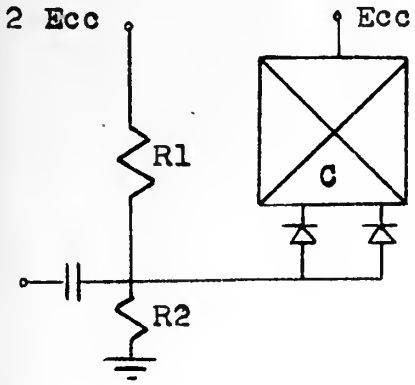
Negative trigger to non-conducting base



Positive trigger to conducting base



Negative trigger to conduting collector



Positive trigger to non-conducting collector

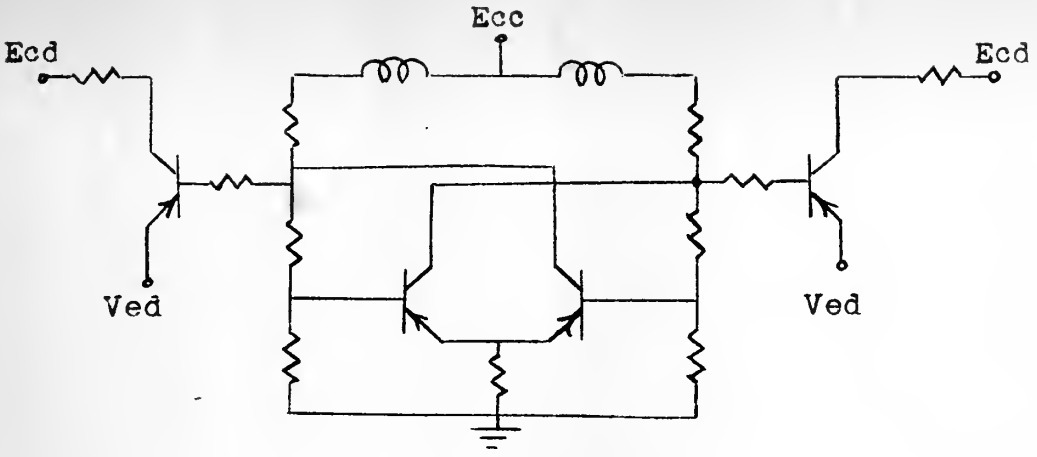
Methods of triggering a p-n-p flip-flop

Figure 10

means of controlling either a voltage or a current load. With transistors a current load is to be expected, even though simultaneous voltage conditions must be met. One method of utilizing the flip-flop to control a transistor driver is indicated in Figure 11. Here Ved is at a voltage level midway between that of Vc-on and Vc-off. If the driver and the flip-flop transistors are of the same type (i.e. all transistors are p-n-p types or all are n-p-n types) current flows in the driver which is connected to the flip-flop transistor which is non-conducting. If the driver is of a different type from the flip-flop transistors, current will flow in the driver while the transistor to which it is connected is conducting. Effects of loading are most easily seen when considered in conjunction with the graphical circuit representation of Chapter IV, and will be considered further there. Use of the inductor in Figure 11 improves driver switching time very noticeably when Ic is large.

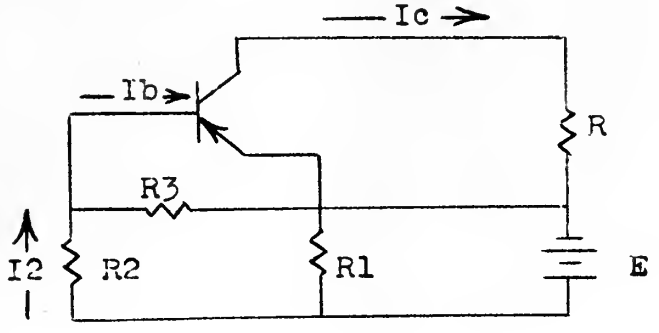
6. Capabilities and limitations.

(a) Frequency of operation of the junction transistor flip-flop is primarily a function of the inherent capability of the particular transistors in use. The equations derived by Ebers and Moll [2] in Figure 3 indicate the parameters of the transistor which are important in determining rise and fall times. These times are directly related to the acceptable maximum frequency as determined by waveshapes. The frequency of alpha cut-off seems to have the greatest importance in determining maximum frequency of operation. It also appears that those



Flip-flop circuit with driver load

Figure 11



A d-c amplifier

Figure 12

units with a higher current amplification factor are capable of higher frequency of operation. In commercial units both of these factors usually improve simultaneously so that it has not been possible to obtain any experimental data in this connection, but it does appear that some gain-bandwidth consideration might be applicable here. The transient settling time of the external circuitry may also place a limitation on the maximum frequency of operation, particularly when various diode gating circuits are used which must recharge to a final level before the circuit can again be triggered.

(b) Power dissipation of the transistors when the circuit is in either of the quiescent states must be within the limitations set by the manufacturer or within a limitation otherwise determined as safe. It is permissible for the operational load line to lie in a position which will take the power dissipation into the excess power regions, but precautions must be taken to ensure that the average power dissipation does not exceed the safe limit.

(c) No particular investigation of environmental effects has been carried out. During the course of experimental work, circuits were operated in temperatures of from twenty to thirty degrees Centigrade with no noticeable effect on circuit performance.

CHAPTER IV

DESIGN METHODS

1. The design problem.

The design problem, as we are concerned here, is the selection of values for Ra, Rb, Rc, Re, and Cl as shown in Figure 4. The selection of these values will be governed by the stability condition of the circuit and by the desired performance characteristics of the circuit.

The stability condition of the circuit has been indicated previously. In the final analysis, the requirement is that the base current in one unit be of sufficient magnitude to cause the other unit to remain non-conducting.

In general there will be several conditions of circuit behavior which might influence design. These might be supply voltages to be utilized, desired voltage swing at the collectors, desired current level in the on state, or any combination of these criteria. In particular, the writer generally has taken as a starting point a particular value of battery voltage and a particular level of current in the conducting collector.

Three methods of design are described below. The shortcomings of each are described in order that a more complete understanding of the problem may be obtained. None is felt to have achieved perfection although the graphical method presented most nearly achieves this end.

In this connection, it is well to point out that the graphical method is equally well adapted for analysis of the circuit while the others are not.

2. The elementary approach.

The method described here is the utmost in simplification and approximation. It takes advantage of the fact that with very large values of base current, the transistor has no appreciable effect on the collector current. It represents an excellent demonstration of the adaptability of junction transistors to this type of circuit, but leaves much to be desired in ultimate design control and in prediction of effects of variation of parameters. There is no possibility of using this approach in design of a circuit which never reaches the saturation current level. The method as given was described by Stanley Schenkerman in "Design of Junction Transistor Trigger Circuits" [9].

Assumptions:

(1) Both transistors have similar characteristics,
(2) J1 is on, J2 is off, (Figure 4 applies)
(3) Base loading of the off transistor is negligible,
(4) Alpha is unity.
  (a) $V_{eb\text{-}on} \geq 0$ (will actually be zero)
  (b) $V_{eb\text{-}off} < 0$
  (c) $|V_{b\text{-}on}| \geq |V_e| > |V_{b\text{-}off}|$
  (d) $V_{c\text{-}out} = V_{c\text{-}off} - V_{c\text{-}on}$
  (e) $V_{c\text{-}off} = E_{cc}$
  (f) $V_{c\text{-}on} = E_{cc} - I_cR_c$
  (g) $V_{b\text{-}off} = \left[\frac{R_b}{R_b + R}\right] V_{c\text{-}on}$
  (h) $V_{b\text{-}on} = \left[\frac{R_b}{R_b + R}\right] V_{c\text{-}off}$
  (i) $V_e = I_cR_c$

An example is given in the reference which serves primarily as an emphasis of the limited utility of this method as a means of precision control.

3. The d-c amplifier approach.

In an effort to obtain a more precise and predictable method of design than was afforded by any of the variations of the elementary approach, the circuit was regarded as a cascaded d-c amplifier with all of the output fed back to the input. The general results of this approach were good, although attempts to load the circuit showed that it still did not provide the degree of flexibility desired. The use of an arbitrarily selected design factor was found to be annoying and led to computation of several sets of values for each set of conditions with selection of the particular values to be used left until after examination of resulting voltage swings, etc. All in all the method is accurate but laborious and slow. It is a good demonstration of the validity of the assumption that the circuit acts as an amplifier, which may become important in analysis of the circuit.

This method is based upon bias stabilization equations derived by R. F. Shea in "Principles of Transistor Circuits" [8] on pages 102 and 103. The circuit that Shea uses is shown in Figure 12. Assumptions made are that alpha is constant over the operating range, that the voltage drop from emitter to base is negligible, and that the collector to base voltage is held within the region where it has little effect upon the collector current. After writing and solving

conventional mesh equations, Shea defines "S" as the stability factor; it is the ratio of change in Ic to that in Ico. The equations finally derived by Shea are:

$$S = \frac{\partial I_c}{\partial I_{co}} = \frac{1 + R_1/R_2 + R_1/R_3}{1 - \alpha + R_1/R_2 + R_1/R_3}$$

$$R_1 = \frac{\alpha (E - R_2 I_c - V_{ce})}{I_c - I_{co}}$$

$$R_3 = \frac{E(S-1)}{I_c - S I_{co}}$$

$$R_2 = \frac{R_1 R_3 (S-1)}{R_3 S \alpha - (S-1)(R_1 + R_3)}$$

Note that the equation for R3 will become the equation for Ra plus Rc when adapted for application to the basic flip-flop of Figure 4. For our purpose, it will generally be possible to neglect Ico as compared to Ic and when this is done, the equations may be reduced to the form given below. R2 was reduced to the simplified form given by direct substitution.

$$R_1 = R_e = \alpha \left(\frac{E - R_c I_c - V_{ce}}{I_c} \right)$$

$$R_3 = R_a + R_c = E/I_c\ (s-1)$$

$$R_2 = R_b = Re/\alpha \left(\frac{1}{\frac{R_c I_c}{E(s-1)} - \frac{1}{\beta}} \right)$$

It is seen that no provision for selection of Rc has been made here. It will be necessary to select Rc from a knowledge of Ecc and the desired collector current in the on transistor, or from some equivalent restriction upon the operating conditions. It is feasible to use these equations for either a saturating or a non-saturating condition of transistor operation, depending upon the value selected for Vce, which is the drop from collector to emitter.

4. The graphical technique.

In an effort to eliminate some of the tedium of the procedure, to obtain precision control of loading, to allow rapid and easy determination of effects of variation of parameters, and to facilitate a "feel" for the circuit, a graphical representation of the circuit has been developed. The representation is based principally upon Ohm's Law whereby a physical value of resistance in a circuit may be presented on an E-I plane as a straight line which subtends a voltage equal to the voltage drop across the resistor, and a current equal to the current flowing in the resistor. Voltage drops through a "black box" (such as a transistor) may be presented as displace-

ments along the voltage axis. Current sources may introduce a current at any resistor junction point, and the effect of such a current source is to cause a displacement of the resistor line end points parallel to the current axis.

Figure 13 is a general graphical representation of the circuit of Figure 4. It is seen that resistance values may be expressed as El minus E2 divided by I; where El is the voltage at the high potential end of the resistor and E2 is the voltage at the low potential end of the resistor, and I is the current through the resistor. The expressions below are the same when taken from either Figure 4 or Figure 12, thus the equivalence is indicated.

$$R_c = \frac{E_{cc} - (V_e + V_{ce})}{I_c}$$

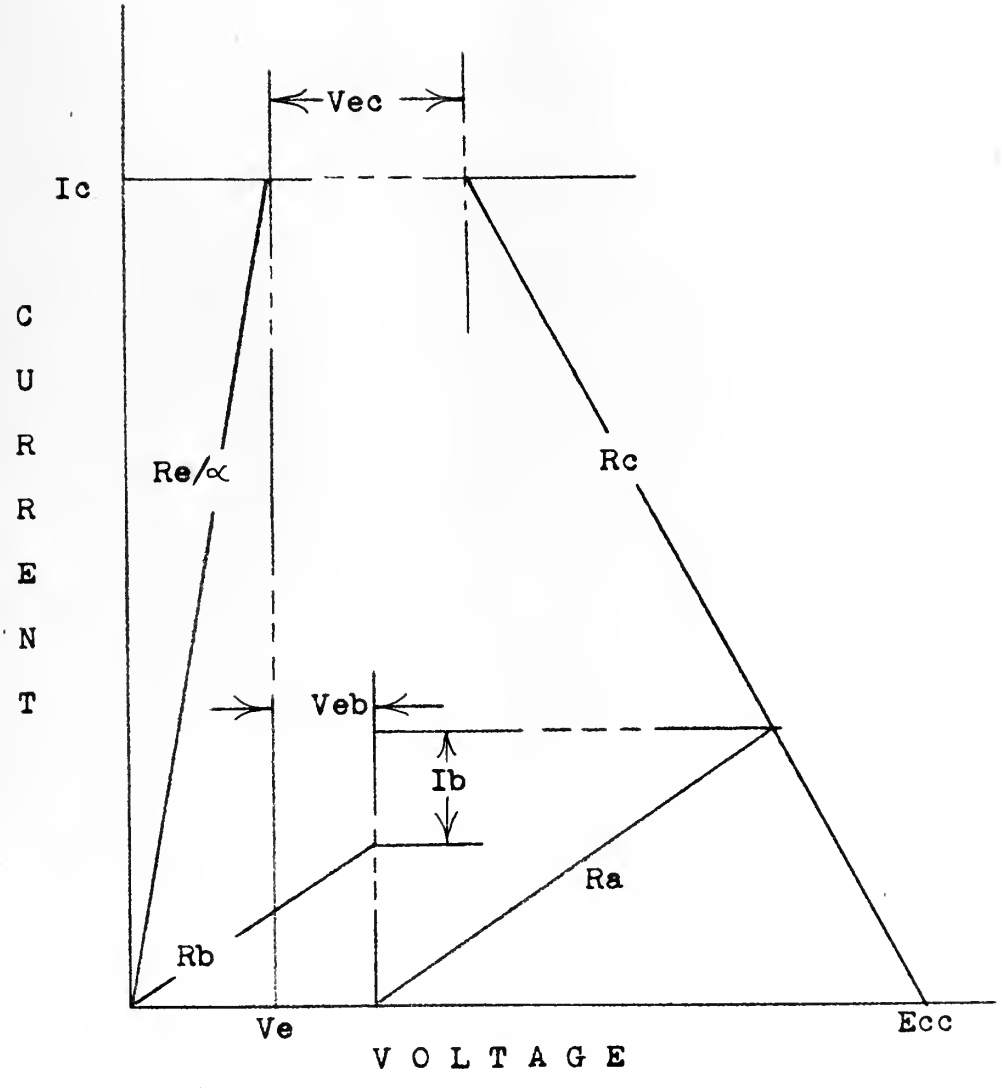
$$R_e = \alpha\left(\frac{E_{cc} - R_c I_c + V_{ce}}{I_c}\right) = \alpha\left(\frac{V_e}{I_e}\right)$$

$$R_a = \frac{E_{cc} - (R_c I_{co} + V_e + V_{eb})}{I_b + I_{bl}}$$

$$R_b = \frac{V_e + V_{eb}}{I_{bl}}$$

Re divided by alpha appears in the diagram since alpha is the ratio of collector to emitter current.

An example of circuit design will be given as an indication of



A graphical representation of the flip-flop

Figure 13

how the method might be used. It is not intended to imply that this is the only way of using the method, or even the best. The procedure will necessarily vary depending upon the initial information and the requirements of the circuit. In any event, the final diagram will have the characteristics of Figure 13.

5. Example: Graphical design method.

Specifications:

Transistor	:	CK 762
Ecc	:	-10½ volts
Ic-on	:	4 milliamperes
Vc-on	:	2 volts

Procedure: (Refer to Figures 14 and 15)

(1) Construct E-I scales to include required values.

(2) Draw vertical construction line at 2 volts (Vc-on) Vce will be assumed to be zero and the circuit will be operated into saturation. Thus, Ve and Vc-on are the same.

(3) Draw horizontal line at level of Ic-on.

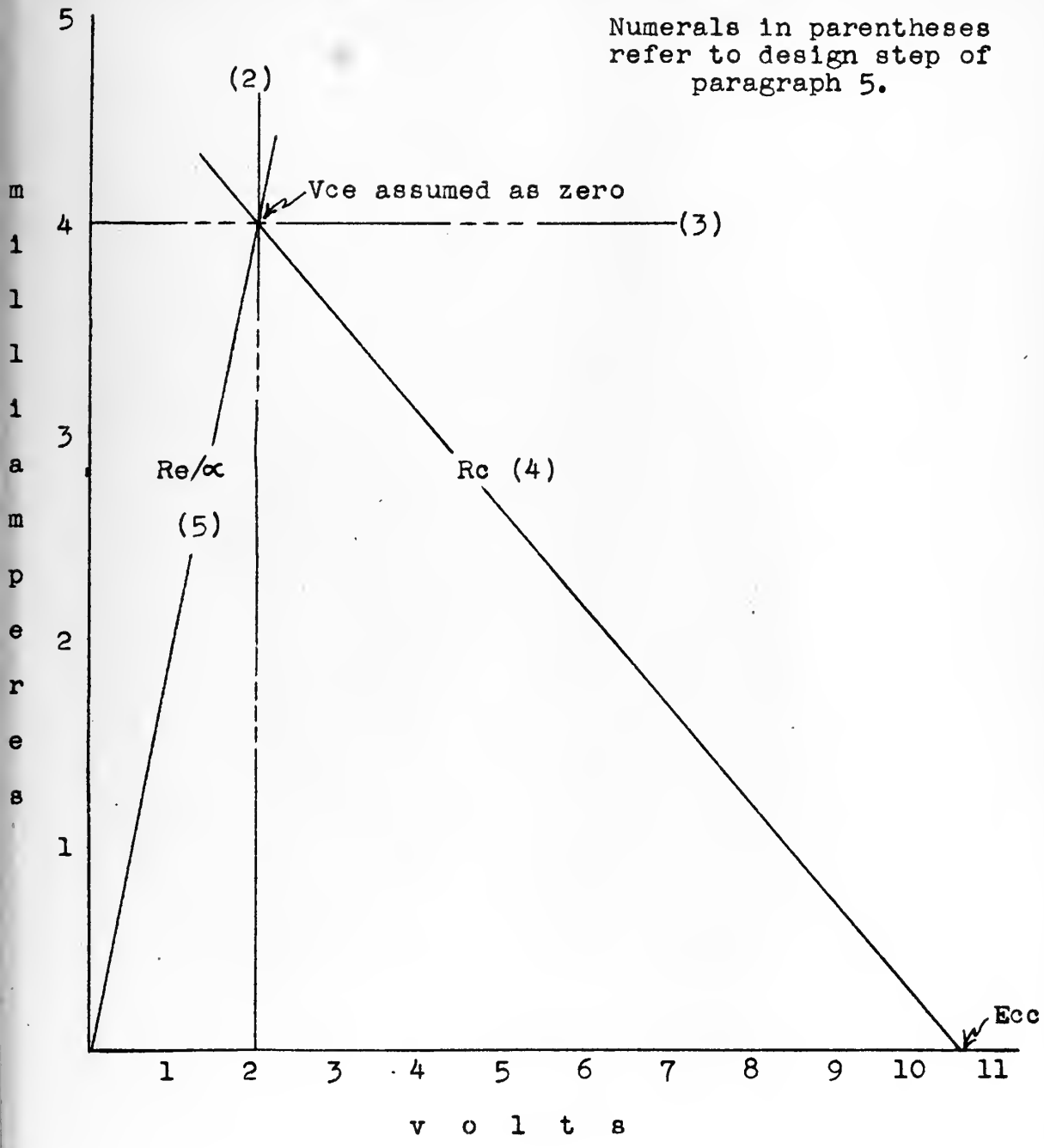
(4) Draw Rc from intersection of (2) and (3) to the voltage axis at Ecc.

(5) Draw Re/α from the origin to intersection of (2) and (3).

(6) Draw a vertical construction line to the right of Ve by an amount Veb. (Figure 15)

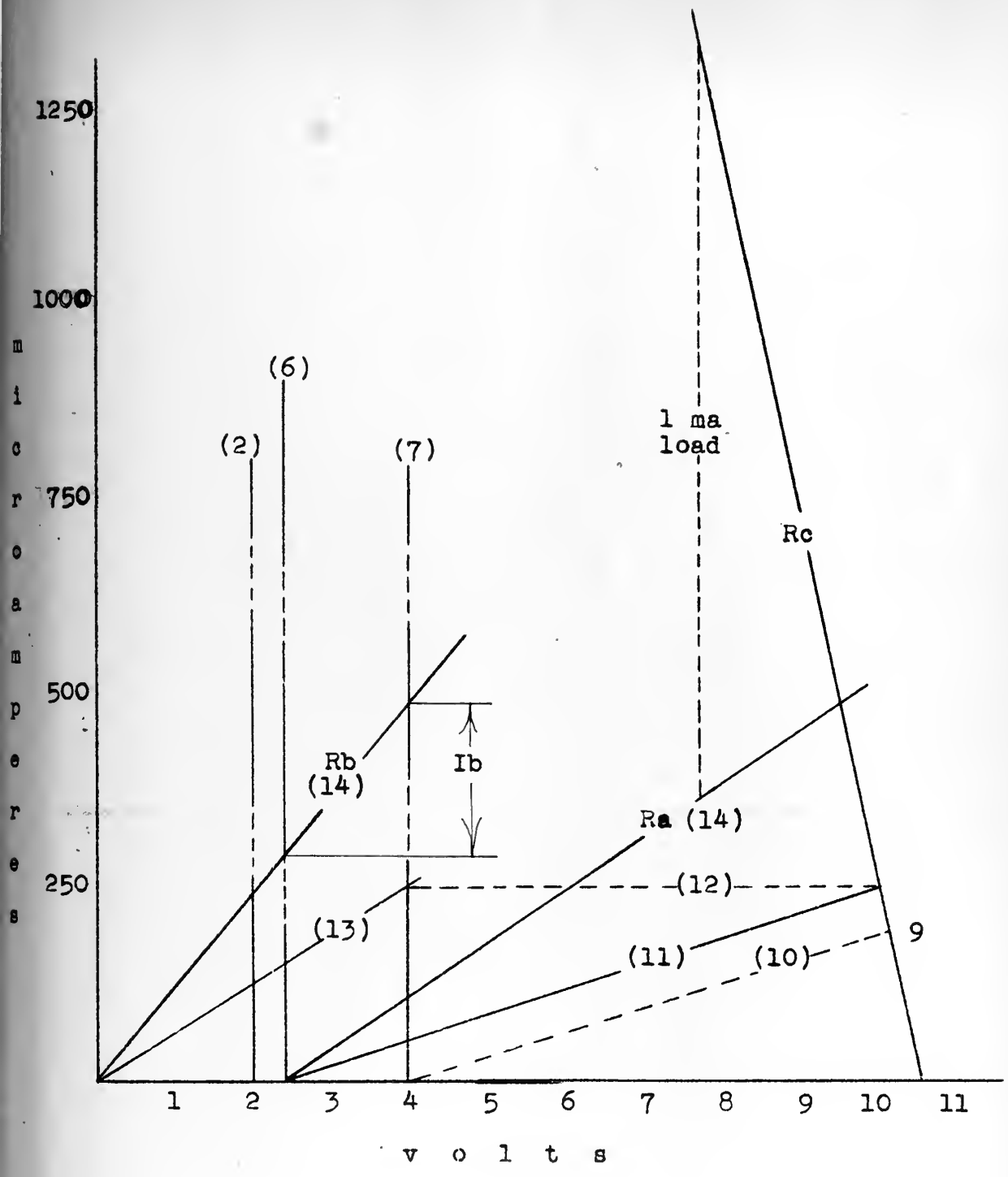
(7) Draw a vertical construction line to the right of Ve by an arbitrary amount. Usually two or three volts will be convenient.

(8) By reference to the collector characteristics the required value of base current is determined. In this case, 90 microamperes of base current will cause collector current to just reach the saturation level. By using 180 microamperes of base current,



Example design

Figure 14



Example design (cont.)

Figure 15

the d-c base current amplification factor might be allowed to decrease by a factor of two before any effect is noted in the circuit.

(9) Note the intersection of the current level selected in (8) with the line representing Rc.

(10) Lay off (do not draw) a line from the point determined by zero current and the voltage of (7) to the point of (9).

(11) Shift the line of (10) parallel to itself, to the location such that it passes through the point determined by (6) at zero current. This line represents a trial value of Ra and is drawn to intersect Rc.

(12) Project horizontally from the intersection of (11) and Rc to the construction line (7).

(13) Draw a line from the origin to the point determined in (12).

(14) The value of base current which would exist with these values of resistance in the circuit is determined as the difference in current levels of the point determined by the intersection of Rb (13) with the line of (6) and the current level used in (9). This value will be smaller than the desired value by some factor. Increase the current of (9) by this factor and repeat the procedure from (9) on, using this new value of current. The final value of Ib is indicated and is seen to be of the desired value.

The effect of a change of battery voltage may be noted at this point. Since all of the resistance lines are straight lines, and all resistance line intersections determine pertinent currents, it is seen that if the voltage, Ecc, reduced by some factor, the currents flowing and the intermediate voltages are reduced by the same factor. The overall result is that variations in battery voltages have very little effect on circuit performance. For one circuit, operation was observed

to be consistent over a range of battery voltage from one and one-half volts to 22.5 volts. Some variation in trigger amplitude was required to give optimum results.

An immediately apparent method of determining effects of resistor variation from the plotted value is the replotting of any or all values of resistance with any percentage of variation. The result would be a diagram of wedges. Extreme limits of wedge intersections could then be examined for acceptable voltage and current levels.

If the circuit is not to be operated into saturation, the effects of variations in base current amplification factor could be examined by plotting a zone of collector current instead of a single-valued line as was done here.

The effect of a one milliampere load can be observed by plotting a vertical line which subtends one milliampere between the intersections of the line with Ra and Rc. This line is plotted in Figure 15. Effects may be observed to be reduction of Ib to about 60 microamperes, and reduction of Vb-off to 7.7 volts instead of 9.4 volts. This reduction in base current is not tolerable in this instance since it would cause the circuit not to reach saturation, thus raising the value of Vc-on toward the reduced value of Vc-off. If it be essential that a one milliampere load be allowable it will be necessary to redesign the values of Ra and Rb.

The values of resistance indicated by the procedure developed above were determined and the circuit was constructed. Diagram values

and the values used are indicated below in that order:

Rc	2150 ohms	2200 ohms
Re	480	470
Rb	8200	8200
Ra	14.3 Kohms	15 Kohms

Voltages from the diagram and as measured in the circuit:

	Diagram	Circuit
Ecc	10.5 volts	10 volts
Ve	2	2
Vc-on	2	2
Vc-off	9.4	8.9
Vb-on	2.4	2.2
Vb-off	.9	1.2

Waveforms of this circuit are shown in Figures 7, 8, and 9 as discussed earlier. Sensitivity curves are given in Appendix I.

6. Selection of speed-up capacitors.

Up to this time no consideration has been given to the selection of C1. Appendix II is an approximate solution to the transient behavior of the circuit. One result of this solution is an indication of the time constant with which C1 is associated. This time constant was found to be:

$$\tau = \frac{R_a + R_b + R_c}{C R_a (R_b + R_c)}$$

This time constant enters into the transient behavior in the rise and

fall times of the circuit, and in order for the circuit to recover in one half the period of a particular state, it is necessary that C1 be chosen to make no larger than the steady state period divided by ten. Large values of C1 tend to reduce the trigger sensitivity, but there is a definite minimum value, which has not been determined, but below which the circuit will not switch. Generally, values of several hundred micro-micro farads was used in experimental work. As an experimental procedure it was found to be desirable to start with an excessively large value of C1 and after the circuit proved to be operative to reduce to an optimum value by experimental observation of collector voltage waveforms.

CHAPTER V

CONCLUSIONS

As a result of the study from which this paper resulted, the following general conclusions and observations have been drawn.

(1) The junction transistor flip-flop is a circuit with a high degree of designability and predictability.

(2) Good, reliable commercial circuitry is practicable now, and better performance is to be expected in the immediate future with continued transistor development.

(3) Further knowledge of the circuit, with consequent improvement in design criteria, is to be expected as a result of an improved theoretical analysis. The articles by Tillman [10] and Reich [7] contain analyses of vacuum tube circuits which might prove of use in determining methods of approach for this analysis.

(4) "A Graphical Method of Flip-Flop Design" by Johnson and Ratz [5] concerns a graphical design technique for vacuum tube circuits which is entirely different from the method described here. It might provide a point of departure for further study of the transistor circuit.

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APPENDIX I

TRIGGER SENSITIVITY

No quantitative solution of trigger requirements for the junction transistor flip-flop has been obtained. All of the circuits investigated had similar characteristics as far as trigger requirement variations are concerned.

The curves following are the result of measurement of trigger requirements for the CK 762 circuit used as a design example in Chapter IV. Variations of voltage and current required at different trigger widths are shown for two frequencies.

The current in the trigger pulse was determined by insertion of a 1000 ohm resistor in series with the trigger source and measurement of the voltage drop across the resistor. Voltage measurements were made by use of a Techtronix oscilloscope.

Thesis (MS) U. S. Naval Postgraduate School, 1955.

Trigger current and voltage vs. Trigger width
at 150 KC and 50 KC

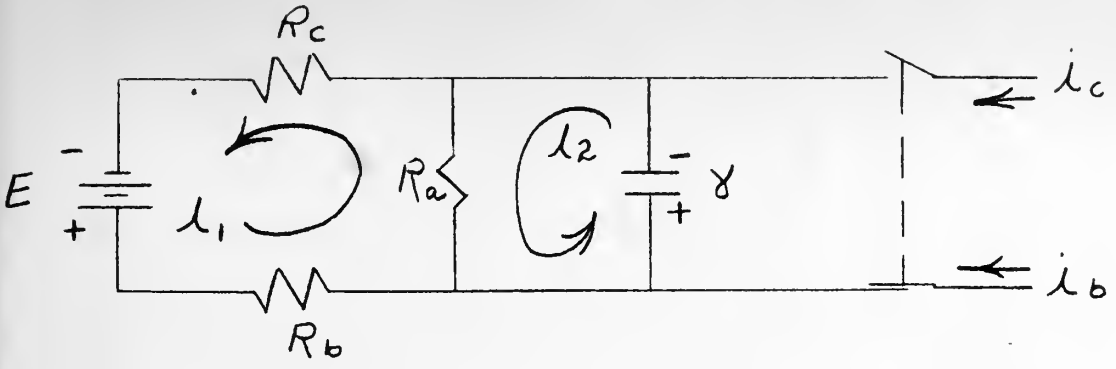
APPENDIX II

TRANSITION OF THE JUNCTION TRANSISTOR FLIP-FLOP

An effort has been made to determine an expression for the variation of base and collector voltages during the transition intervals. The solution is indicated and the resulting expressions are given. A plot of calculated results for one circuit is given and compared to the observed waveform.

Two approximations were made in arriving at the solution which are too severe to give good results throughout. First, a truly exponential increase in collector current was assumed, while actually the current is not exponential since the base circuit changes are neither a unit step of voltage nor a unit step of current. Second, an instantaneous interruption of base current in the unit turning off was assumed, while actually the current might even reverse to an appreciable value before being reduced to Ibo. It may be that a much more elaborate approach will be required to include these effects to the required accuracy.

It is felt that improved circuit design criteria might result from a good solution of the transition interval. A further result might be an improvement in transistor specifications for the circuit.



$$E = (R_a + R_b + R_c) i_1 - R_a i_2 + R_c i_c$$

Let $E - R_c i_c = E'$

$$E' = (R_a + R_b + R_c) i_1 - R_a i_2$$

$$-\gamma = -R_a i_1 + \left(R_a + \frac{1}{Cp}\right) i_2$$

Taking La Place Transforms

$$E'/s = (R_a + R_b + R_c) I_1 - R_a I_2$$

$$-\gamma/s = -R_a I_1 + \left(R_a + \frac{1}{Cs}\right) I_2$$

$$I_1 = \Delta_{11}/\Delta = \frac{E' - \gamma}{R_b + R_c} \times \frac{1}{s + \frac{(R_a + R_b + R_c)}{C R_a (R_b + R_c)}} + \frac{E'}{C R_a (R_b + R_c)} \times \frac{1}{s\left(s + \frac{R_a + R_b + R_c}{C R_a (R_b + R_c)}\right)}$$

Inverse transform gives

$$i_1 = \frac{E' - \gamma}{R_b + R_c} e^{-t/\tau} + \frac{E'}{R_a + R_b + R_c}\left(1 - e^{-t/\tau}\right)$$

where $\gamma = \dfrac{R_a + R_b + R_c}{C R_a (R_b + R_c)}$

Similar calculation can be made for switches in opposite positions giving expressions for base and collector voltages. To reach final steady state of:

$$V_{c\text{-}on} = -E + \left[I_c + \frac{E - I_c R_c - \gamma_1}{R_b + R_c} \epsilon^{-t/\tau} + \frac{E - I_c R_c}{R_a + R_b + R_c} (1 - \epsilon^{-t/\tau}) \right] R_c$$

$$V_{b\text{-}off} = \left[\frac{E - I_c R_c - \gamma_1}{R_b + R_c} \epsilon^{-t/\tau} + \frac{E - I_c R_c}{R_a + R_b + R_c} (1 - \epsilon^{-t/\tau}) \right] R_b$$

$$V_{c\text{-}off} = -E + \left[\frac{E - I_b R_b - \gamma_2}{R_b + R_c} \epsilon^{-t/\tau} + \frac{E - I_b R_b}{R_a + R_b + R_c} (1 - \epsilon^{-t/\tau}) \right] R_c$$

$$V_{b\text{-}on} = \left[I_b + \frac{E - I_b R_b - \gamma_2}{R_b + R_c} \epsilon^{-t/\tau} + \frac{E - I_b R_b}{R_a + R_b + R_c} (1 - \epsilon^{-t/\tau}) \right] R_b$$

$$\gamma_1 = V_{c\text{-}off} - V_{b\text{-}on} = -E - \left(\frac{E - I_b R_b}{R_a + R_b + R_c} \right) R_c - \left(\frac{E - I_b R_b}{R_a + R_b + R_c} \right) R_b$$

$$\gamma_2 = V_{c\text{-}on} - V_{b\text{-}off} = -E - \left(\frac{E - I_c R_c}{R_a + R_b + R_c} \right) R_c - \left(\frac{E - I_c R_c}{R_a + R_b + R_c} \right) R_b$$

A computed waveform for $V_{c\text{-}on}$ is compared with the observed waveform

Comparison of computed and observed collector waveforms

28497
K413 Kilpatrick
Some design techniques and considerations for a junction transistor flip-flop.